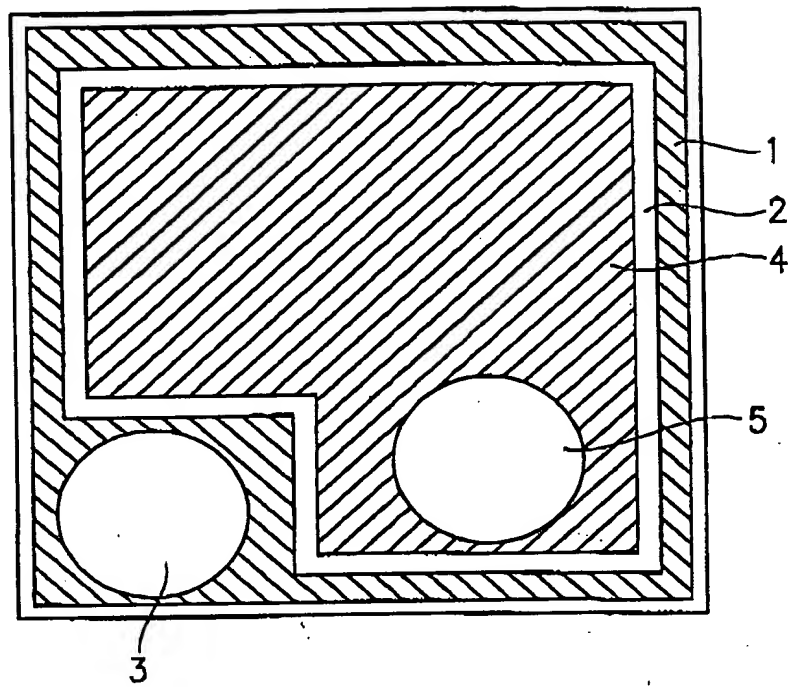
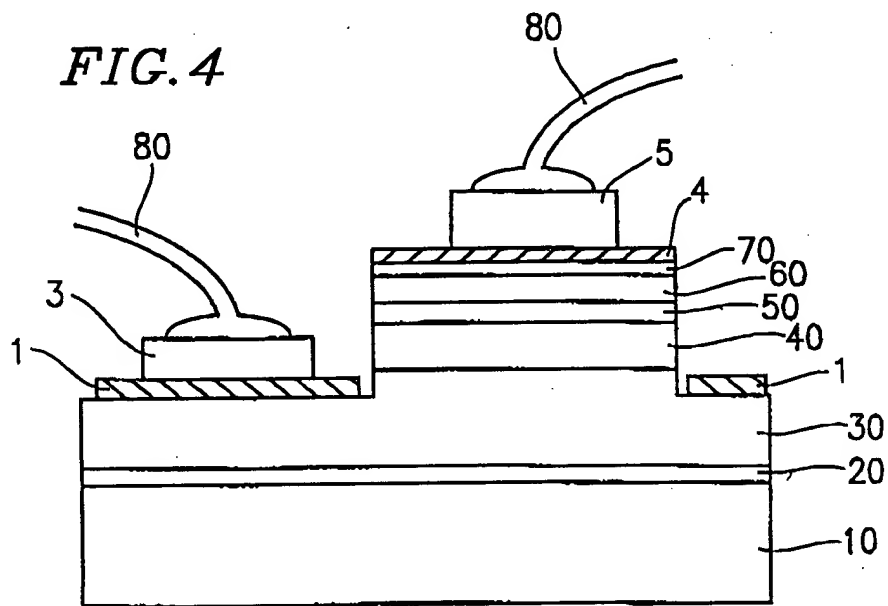


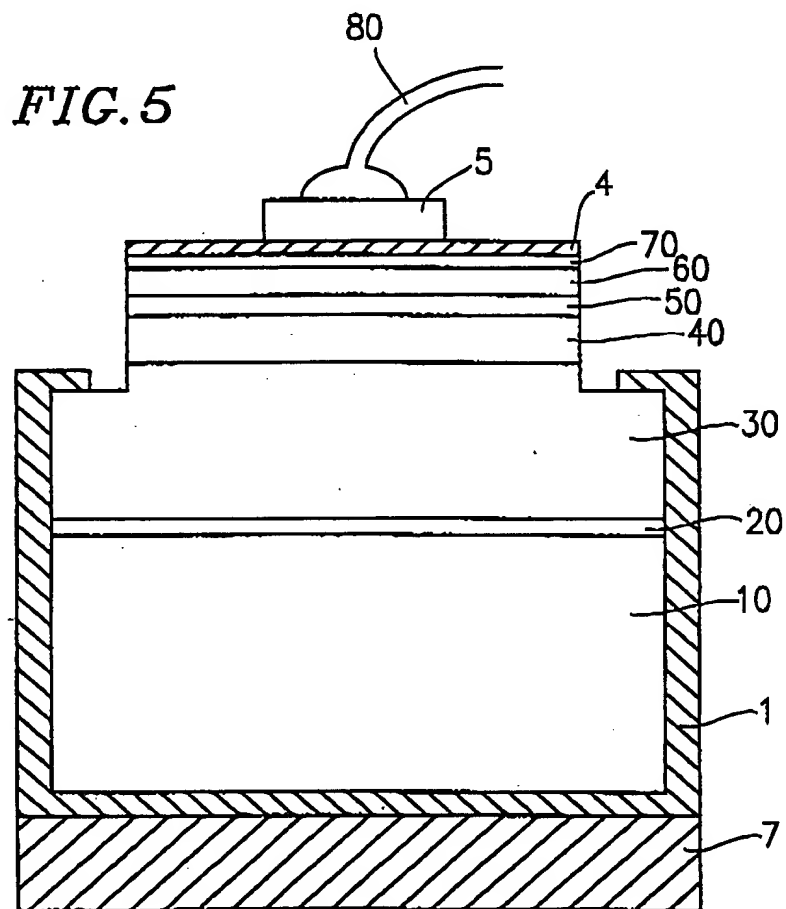
*FIG. 1*1000

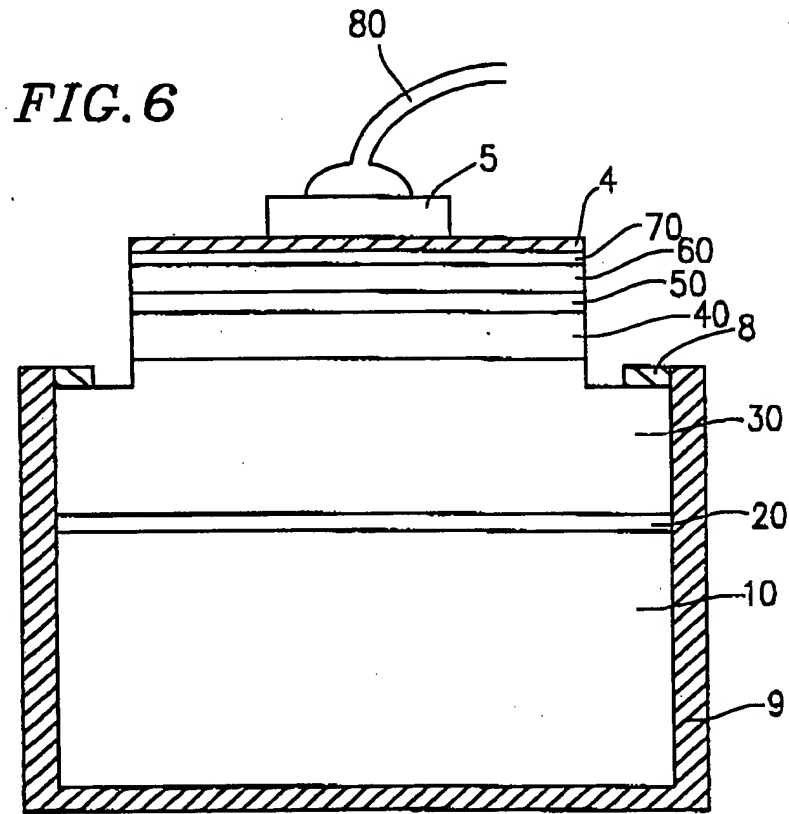
[illegible]

[illegible]

FIG. 4

1000

3000



4000

FIG. 6

FIG. 7

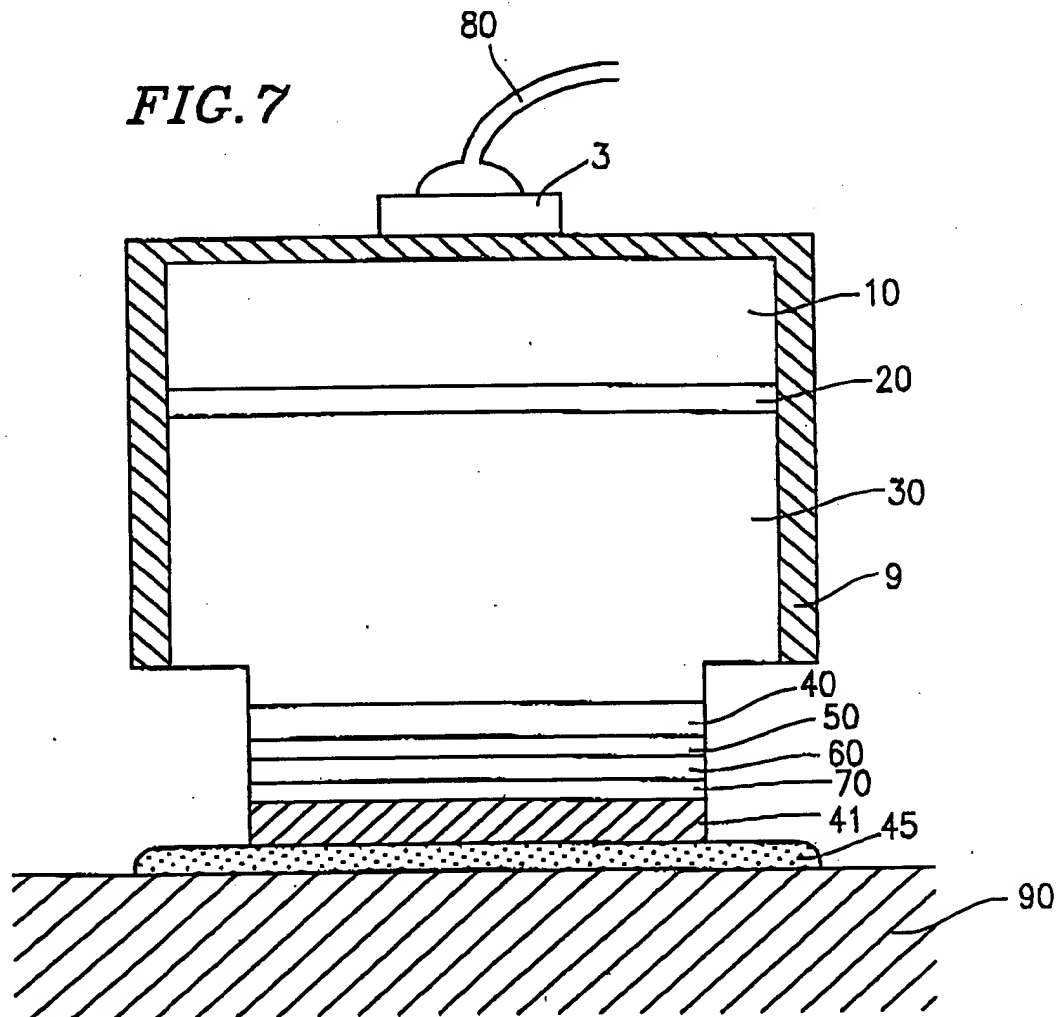


FIG. 8A

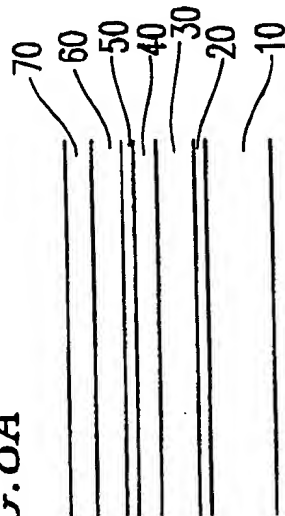


FIG. 8D

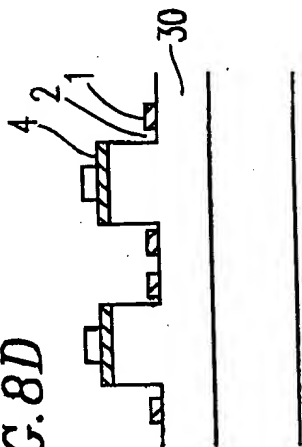


FIG. 8B

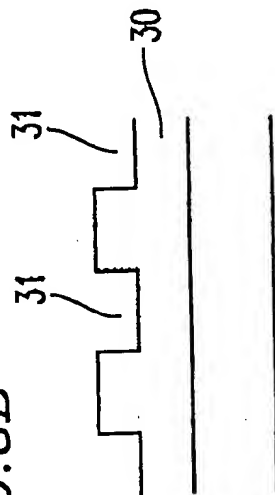


FIG. 8E

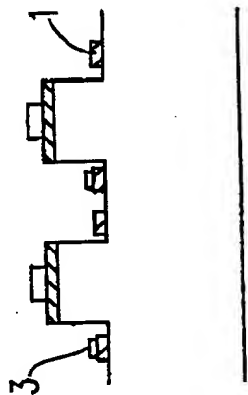


FIG. 8C

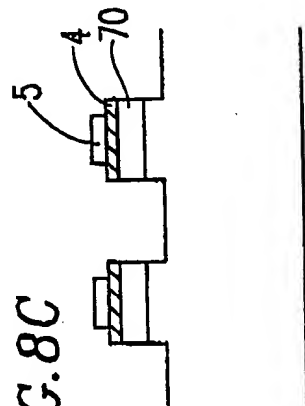


FIG. 8F

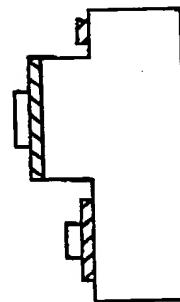




FIG. 9A

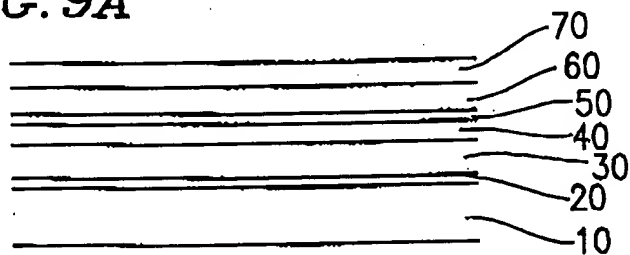


FIG. 9D

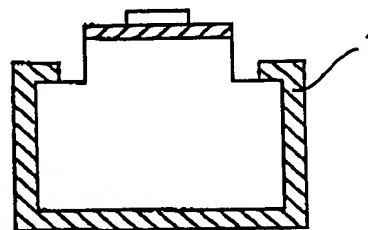


FIG. 9B

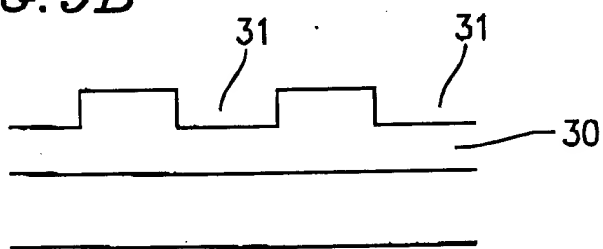
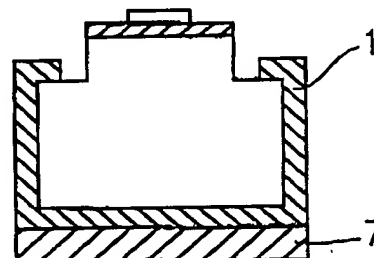
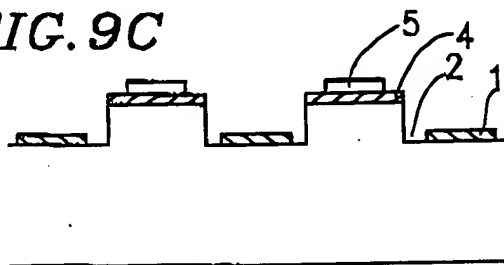


FIG. 9E



3000

FIG. 9C



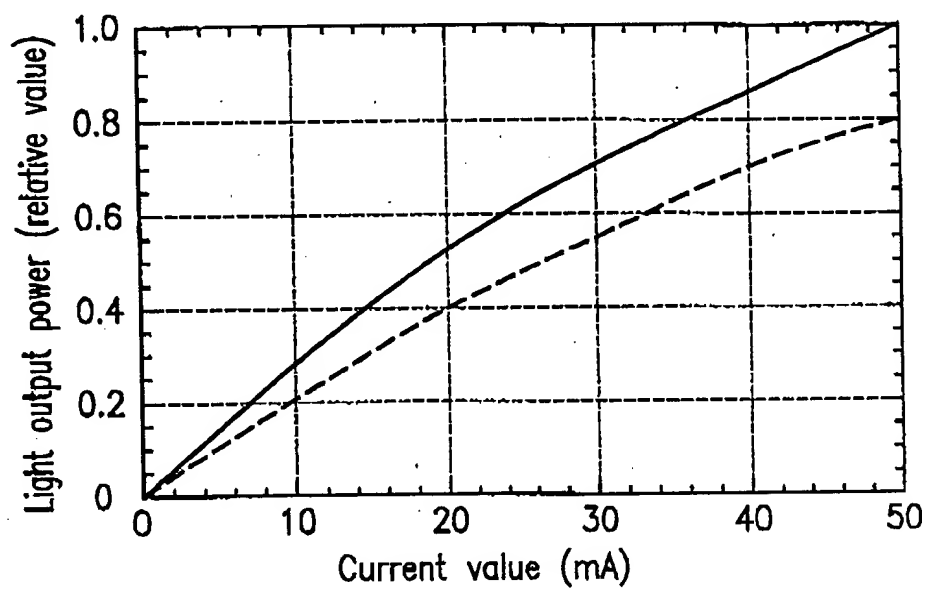
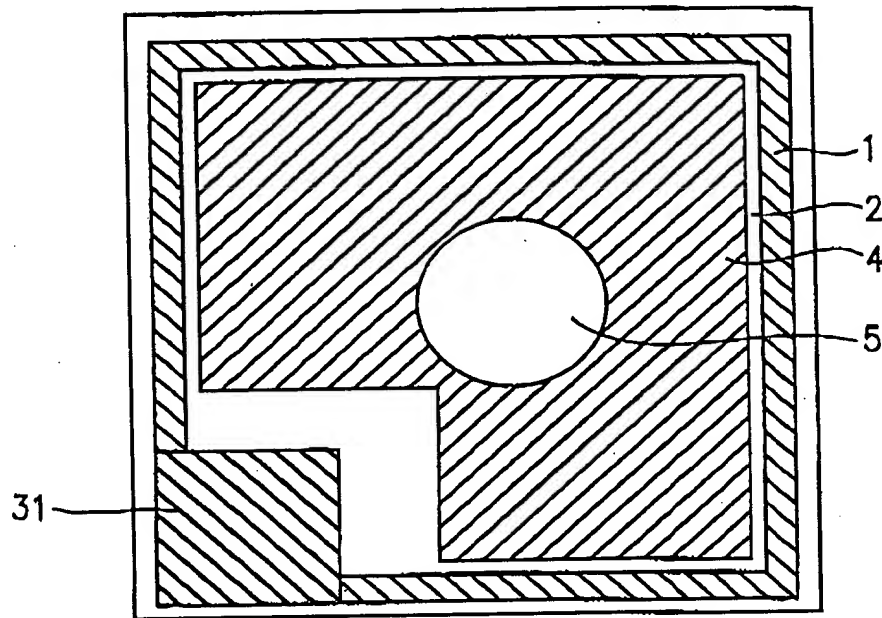
*FIG. 10*

Figure 1 is a schematic cross-sectional view of a semiconductor device. It shows a substrate 1 with a top layer 2. A patterned layer 4 is formed on top of layer 2, featuring a rectangular opening 31 and a circular opening 5. A layer 3 is formed within the rectangular opening 31.

5000

FIG. 12



6000

*FIG. 13*